CLAIMS

What is claimed is:

1. An apparatus comprising:

a duty cycle correction circuit at a receiver in a clock distribution network, the duty cycle correction circuit to correct a duty cycle of a distributed clock signal received at the receiver.

2. The apparatus of claim 1 wherein the duty cycle correction circuit includes

a feedback path between an input and an output of the duty cycle correction circuit, the feedback path to control a delay of a circuit path in the duty cycle correction circuit to correct the duty cycle.

3. The apparatus of claim 2 wherein the duty cycle of a corrected clock signal at an output of the duty cycle correction circuit is substantially equal to 50%.

4. The apparatus of claim 1 further including frequency multiplying circuitry coupled to the duty cycle correction circuit, the frequency multiplying circuitry to receive the distributed clock signal at an input and provide an output clock signal having a frequency that is a multiple of the distributed clock signal.

5. The apparatus of claim 1 further including a smart buffer circuit coupled to the duty cycle correction circuit, the smart buffer circuit to provide for proper operation of the duty cycle correction circuit over a range of loads to be coupled to the duty cycle correction circuit.

6. A clock distribution network comprising:

clock generation circuitry at a first location to generate a global clock signal;

clock distribution circuitry to distribute the global clock signal from the clock generation circuitry to a receiving point at a second, different location; and

a duty cycle correction circuit at the receiving point to correct the duty cycle of the distributed global clock signal received via the clock distribution circuitry.

7. The clock distribution network of claim 6 wherein the clock distribution circuitry is further to distribute the global clock signal from the clock generation circuitry to a plurality of receiving points and wherein each of the plurality of receiving points includes the duty cycle correction circuit.

8. The clock distribution network of claim 7 wherein one of the receiving points further includes frequency multiplying circuitry coupled to the duty cycle correction circuit.

9. The clock distribution network of claim 6 wherein the duty cycle correction circuit includes a feedback path to control a delay of an output clock signal.

10. The clock distribution network of claim 9 wherein a signal communicated via the feedback path in the duty cycle correction circuit controls at least one variable delay element in the duty cycle correction circuit.

11. The clock distribution network of claim 6 wherein the duty cycle correction circuit provides a corrected output clock signal having a 50% duty cycle.

12. A circuit comprising:

an input to receive an input clock signal;

an output to provide an output clock signal having a corrected duty cycle;

a reset path between the input and the output, the reset path to control a width of the output clock signal; and

a feedback path between the output and the reset path to control a delay of the reset path to correct the duty cycle of the output clock signal.

13. The circuit of claim 12 wherein the duty cycle is corrected to a substantially 50% duty cycle.

14. The circuit of claim 13 further including a sense amplifier in the feedback path, the sense amplifier having a threshold substantially equal to one half of a supply voltage (Vcc) to be coupled to the circuit.

15. The circuit of claim 14 wherein each of the reset path and the feedback path is coupled to control a variable delay element.

16. The circuit of claim 12 further including frequency multiplying circuitry coupled to between the input and the output, the frequency multiplying circuitry to multiply the frequency of the output clock signal relative to the input clock signal.

17. The circuit of claim 12 further including smart buffer circuitry coupled between the input and the output, the smart buffer circuitry to provide for proper duty cycle correction for a range of loads to be coupled to the output.

18. An integrated circuit device comprising:

a clock generation circuit to provide a first clock signal having a first duty cycle;

a clock distribution network coupled to the clock generation circuit to distribute the first clock signal across the integrated circuit device; and

a plurality of duty cycle correction circuits at receiving points in the clock distribution network, the duty cycle correction circuits to correct a duty cycle of the first clock signal at the receiving points.

19. The integrated circuit device of claim 18 wherein at least one of the duty cycle correction circuits is coupled to frequency multiplying circuitry.

20. The integrated circuit device of claim 19 wherein the duty cycle correction circuits correct the duty cycle of the first clock signal to be substantially a 50% duty cycle.

21. The integrated circuit device of claim 18 wherein at least one of the duty cycle correction circuits is coupled to smart buffer circuitry to provide for proper operation of the at least one duty cycle correction circuit for a range of loads to be coupled to an output of the at least one duty cycle correction circuit.

22. An apparatus comprising:

a first circuit to provide a first output signal at an output driver, the output driver including a fixed number of devices; and

a smart buffer circuit to match a delay of the output signal to a delay of a reference signal independent of a load coupled to the first circuit over a range of load values, the smart buffer circuit to adjust the delay of the output signal by adjusting the drive strength of the output driver.

23. The apparatus of claim 22 wherein the first circuit is a clock duty cycle correction circuit and the first output signal is an output clock signal.

24. The apparatus of claim 22 wherein the smart buffer circuit includes

a first phase detector to detect a difference in delay between one of a rising or falling edge of the first output signal and a corresponding edge of the reference signal, the first phase detector to provide a first reference control signal at an output, the first reference control signal to control a delay of a first delay element in the first circuit to adjust the drive strength of the driver for a first value of an input signal to the first circuit.

25. The apparatus of claim 24 wherein the smart buffer circuit further includes

a second phase detector to detect a difference in delay between a remaining one of a rising or falling edge of the first output signal and a corresponding edge of the reference signal, the second phase detector to provide a second reference control signal at an output, the second reference control signal to control a delay of a second delay element in the first circuit to adjust the drive strength of the driver for a second value of the input signal to the first circuit.

26. An apparatus comprising:

a duty cycle correction circuit, the duty cycle correction circuit to receive an input clock signal and to generate a reference voltage signal, a voltage of the reference voltage signal to vary in response to a change in frequency of the input clock signal; and

a clock generation circuit to receive the reference voltage signal and to provide an output clock signal, the clock generation circuit to vary the delay of the output clock signal in response to a variation in voltage of the reference voltage signal.

27. The apparatus of claim 26 wherein the clock generation circuit is to provide multiple output clock signals, each of the multiple output clock signals to vary in response to a variation in the voltage of the reference voltage signal.

28. A method comprising:

receiving an input clock signal from a clock distribution network at an endpoint of the clock distribution network; and

correcting the duty cycle of the input clock signal at the endpoint to provide a corrected output clock signal.

29. The method of claim 28 wherein correcting the duty cycle comprises

feeding back the corrected output clock signal to control the correction of the duty cycle.

30. The method of claim 28 wherein correcting the duty cycle comprises correcting the duty cycle such that the corrected output clock signal has a duty cycle substantially equal to 50%.